

FIG. 1
(PRIOR ART)

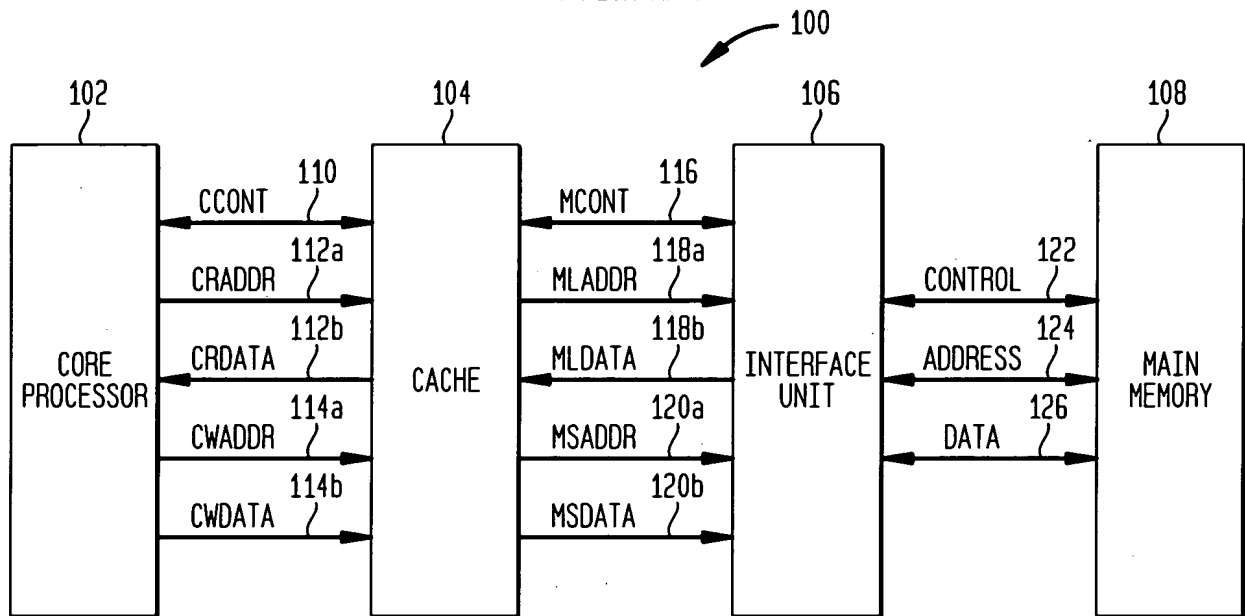


FIG. 2
(PRIOR ART)

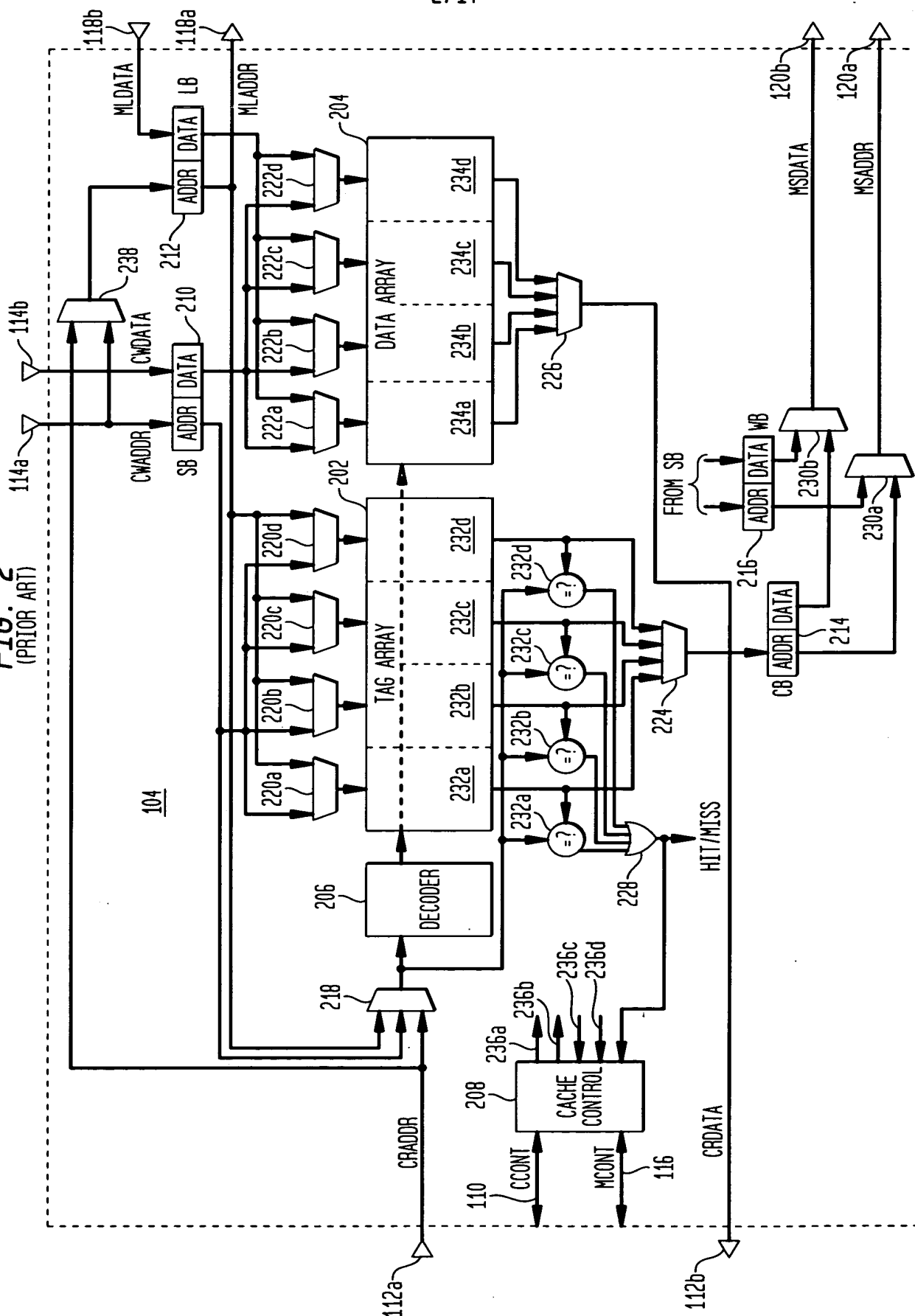


FIG. 3A

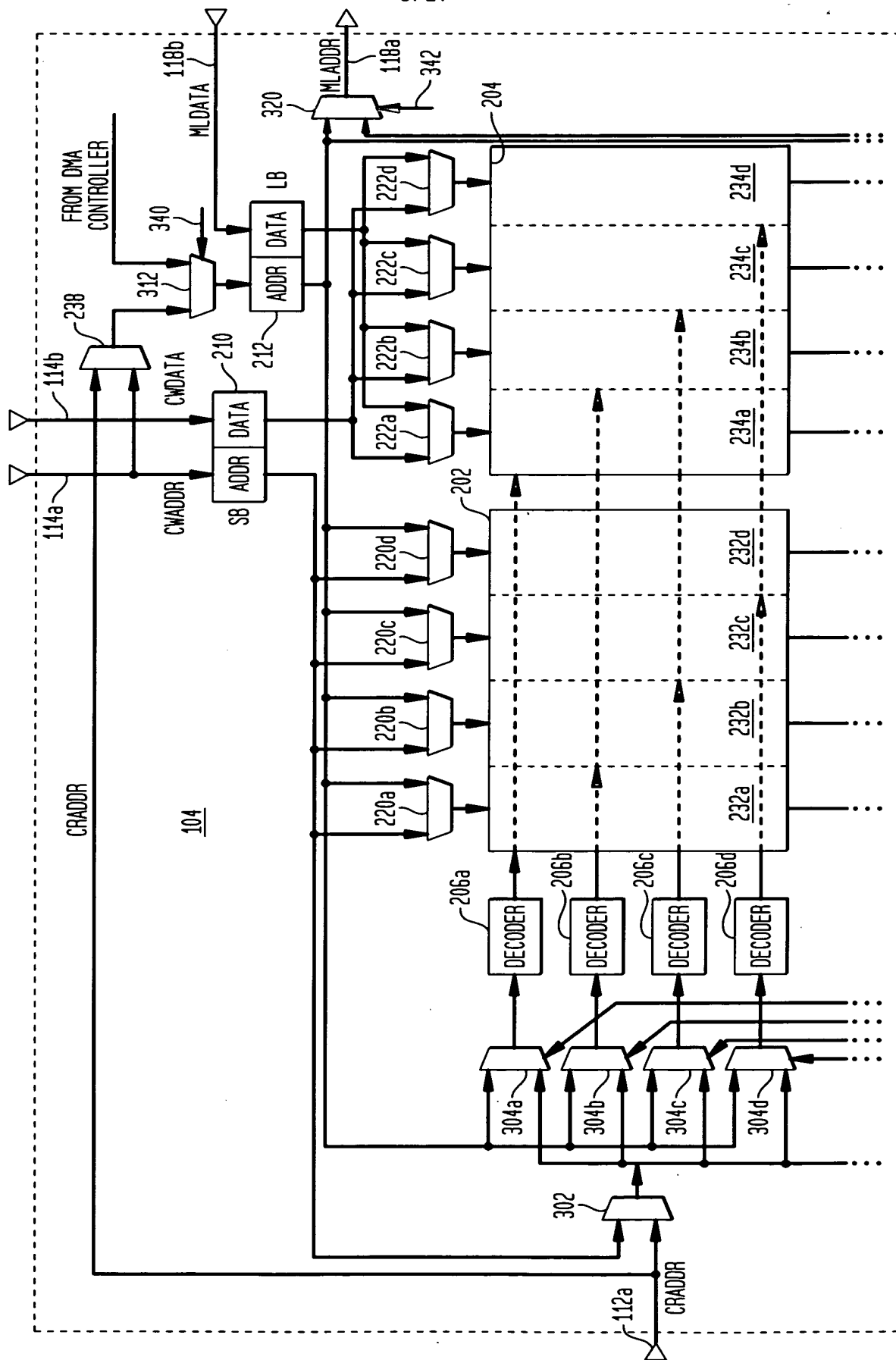


FIG. 3B

FIG. 3B is a detailed block diagram of the system architecture. It shows the following components and their interconnections:

- Cache Controller (208):** Receives **CCONT** (110a) and **MCONT** (115a) signals. It has multiple data paths (324a, 324b, 322a, 322b) connected to the **PRE-LOAD CONTROLLER** (308). It also outputs **HIT/MISS** signals (314a, 314b, 314c, 314d) to the **PRE-LOAD CONTROLLER**.
- PRE-LOAD CONTROLLER (308):** Receives **CCONT** (110c) and **MCONT** (116a) signals. It outputs **TO MUX 312** (342) and **TO MUX 320** (340) signals to the **DMA CONTROLLER** (306).
- DMA CONTROLLER (306):** Receives **CCONT** (110b) and **MCONT** (116b) signals. It has multiple data paths (326a, 326b, 328a, 328b) connected to the **FROM SB** (216) and **WB** (230b) blocks. It also outputs **EADDR** (332) and **IADDR** (344a, 344b, 344c, 344d) signals to the **CR DATA** (112b) block.
- CR DATA (112b):** Receives **EADDR** (332) and **IADDR** (344a, 344b, 344c, 344d) signals. It outputs **CR DATA** (226a, 226b) signals to the **FROM SB** (216) and **WB** (230b) blocks.
- FROM SB (216):** Receives **CR DATA** (226a, 226b) signals. It outputs **ADDR DATA** (214) and **CB** (230a) signals to the **WB** (230b) block.
- WB (230b):** Receives **ADDR DATA** (214) and **CB** (230a) signals. It outputs **WB** (230b) signals to the **DMA CONTROLLER** (306).
- MSDATA (120b) and MSADDR (120a):** These are external data and address buses connected to the **DMA CONTROLLER** (306).

FIG. 4

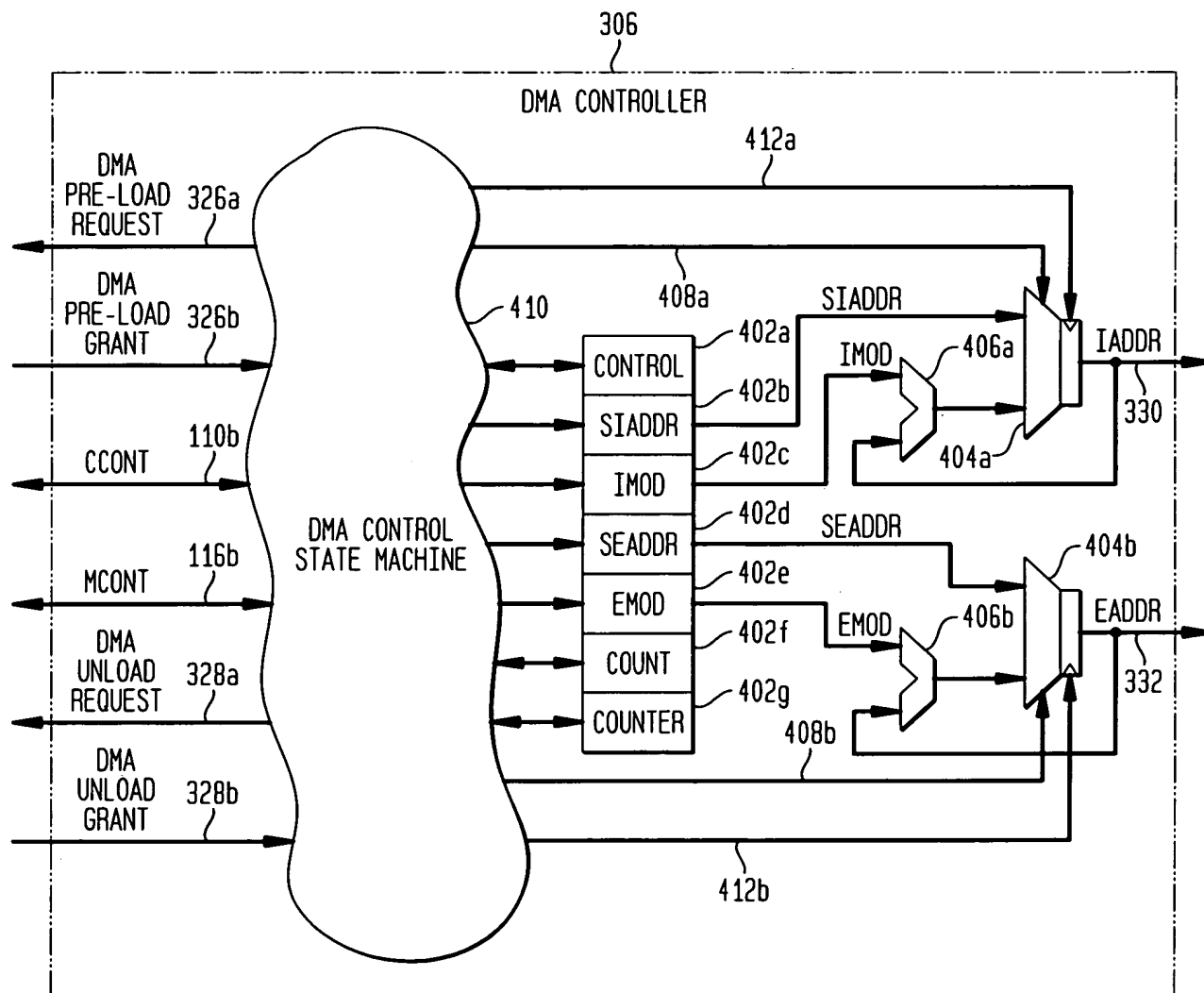


FIG. 5

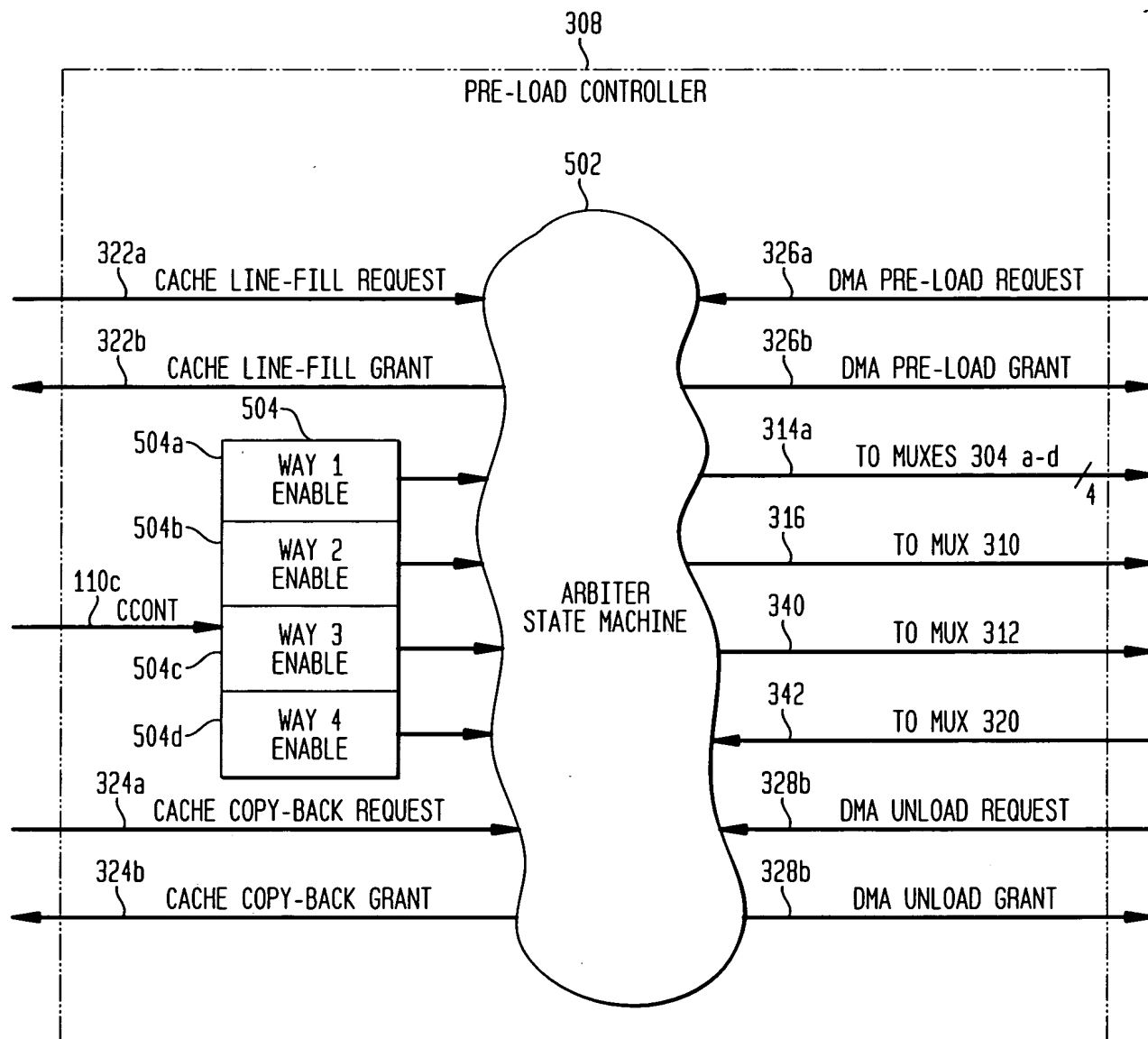
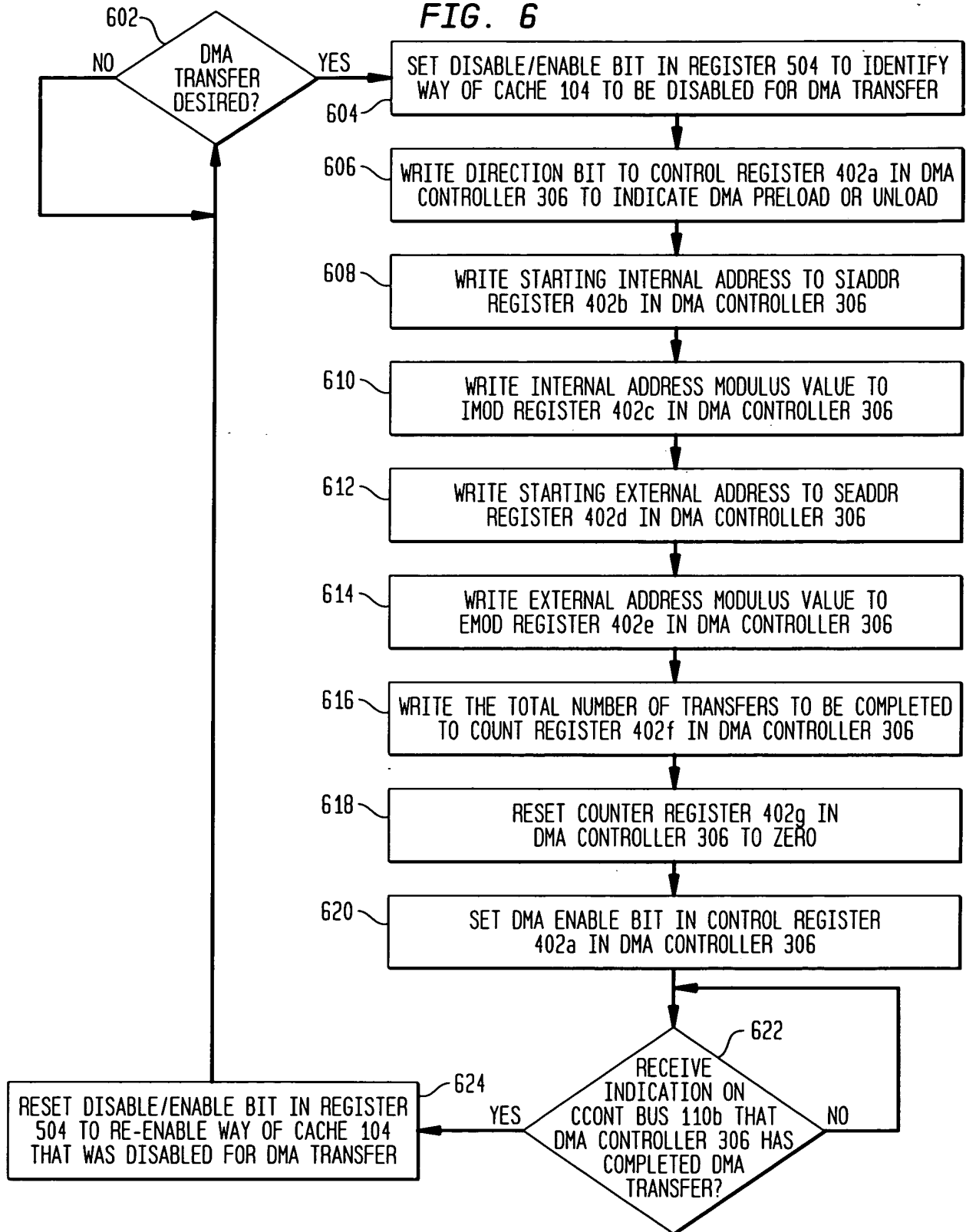
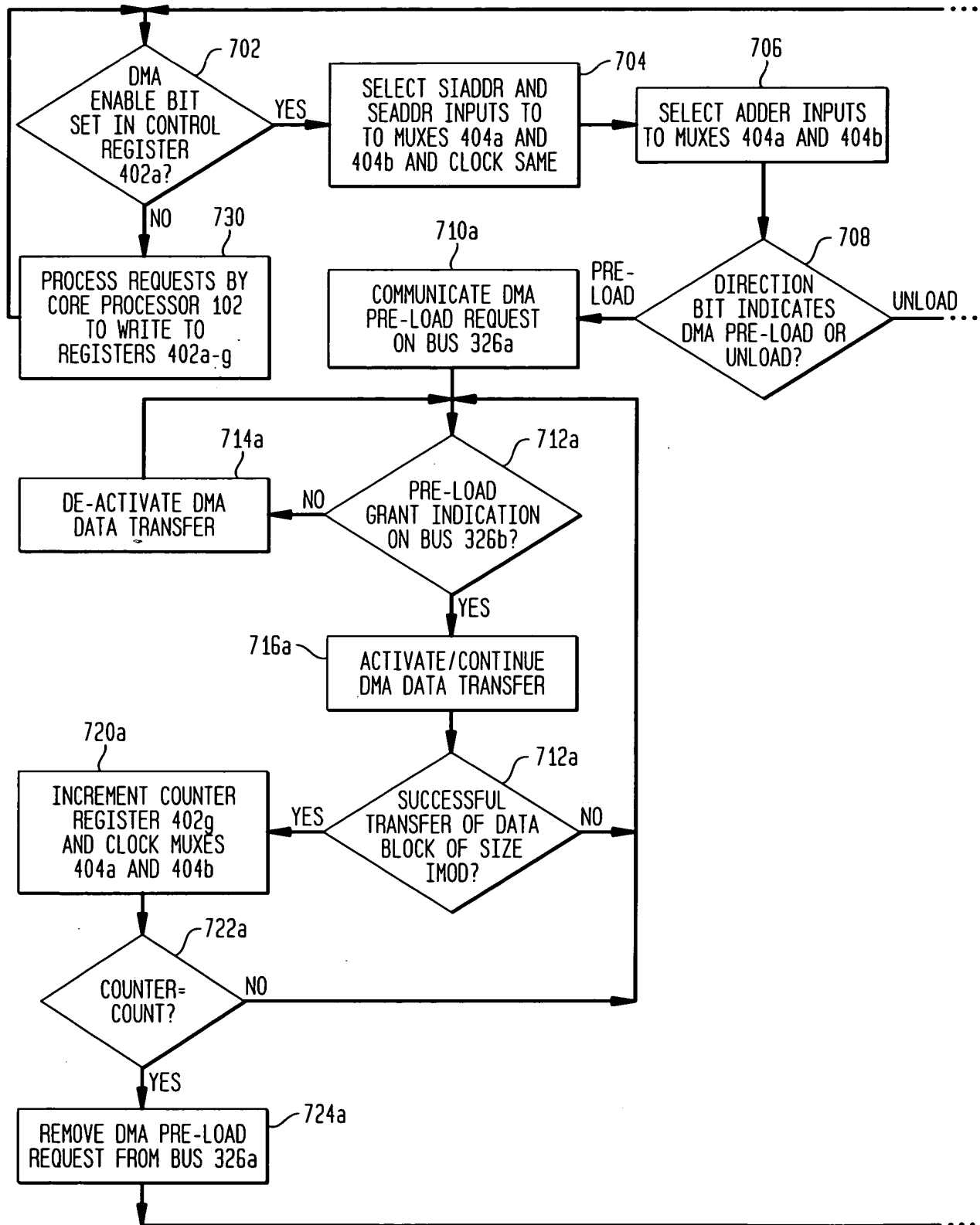


FIG. 6



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FIG. 7A



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FIG. 7B

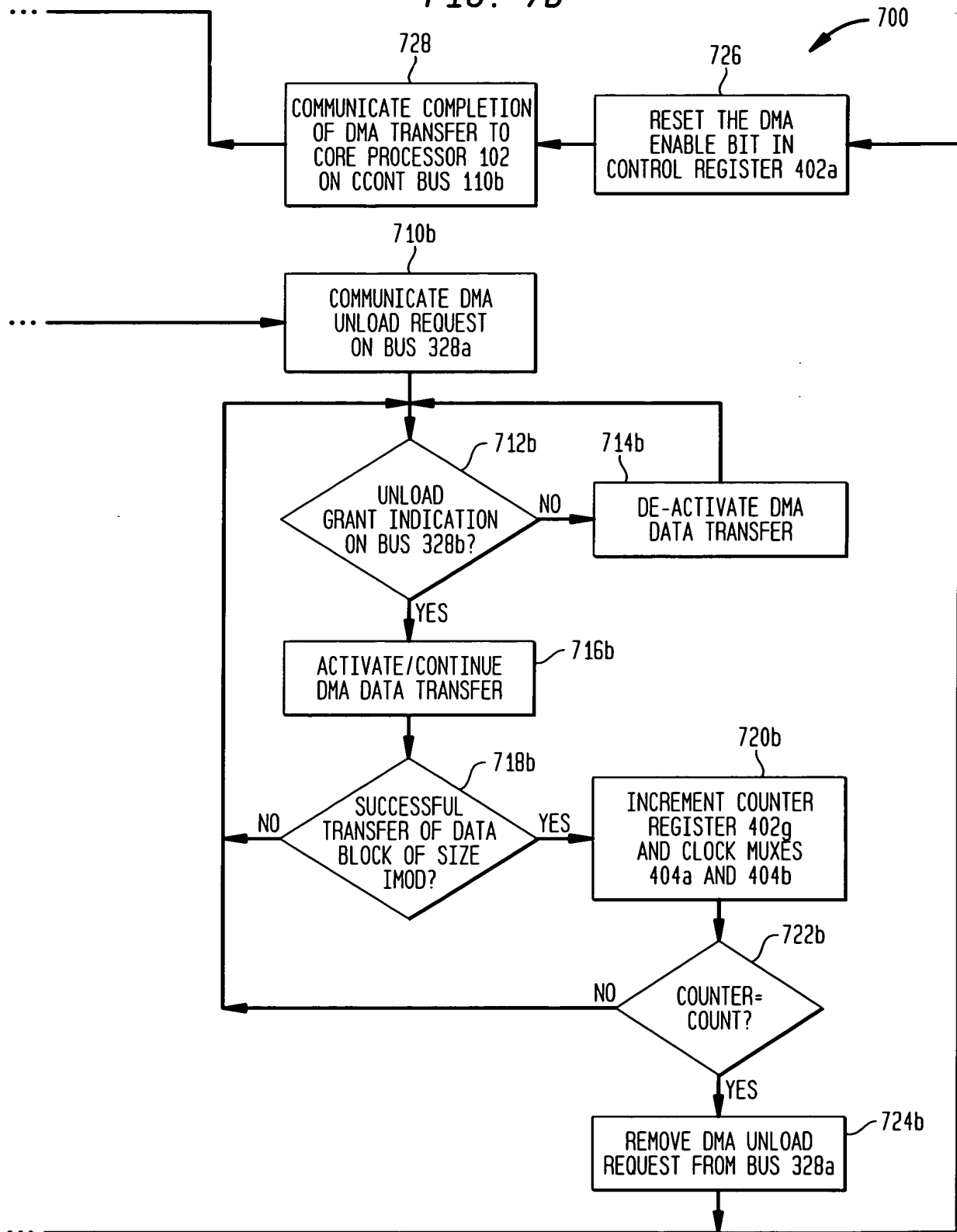


FIG. 8A1

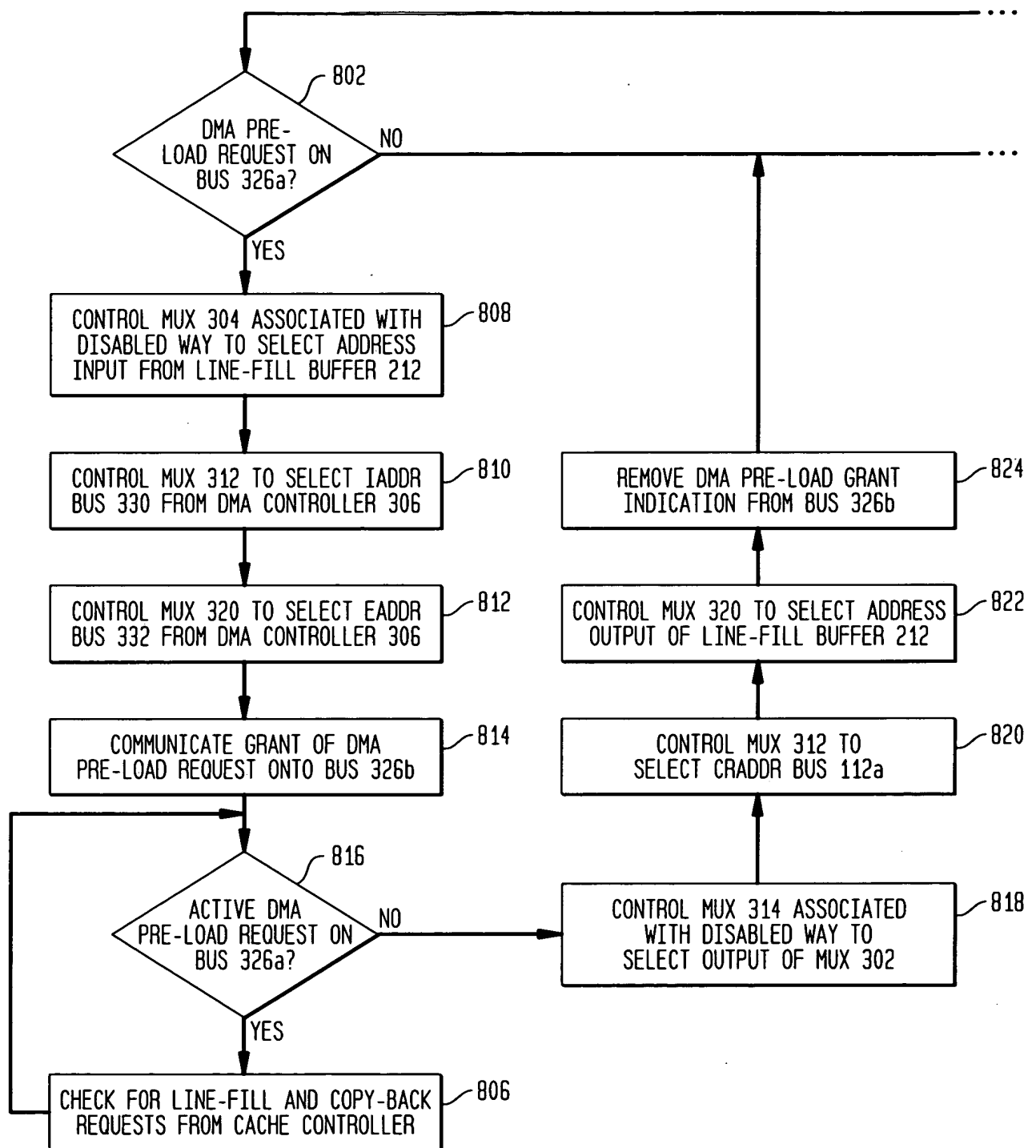
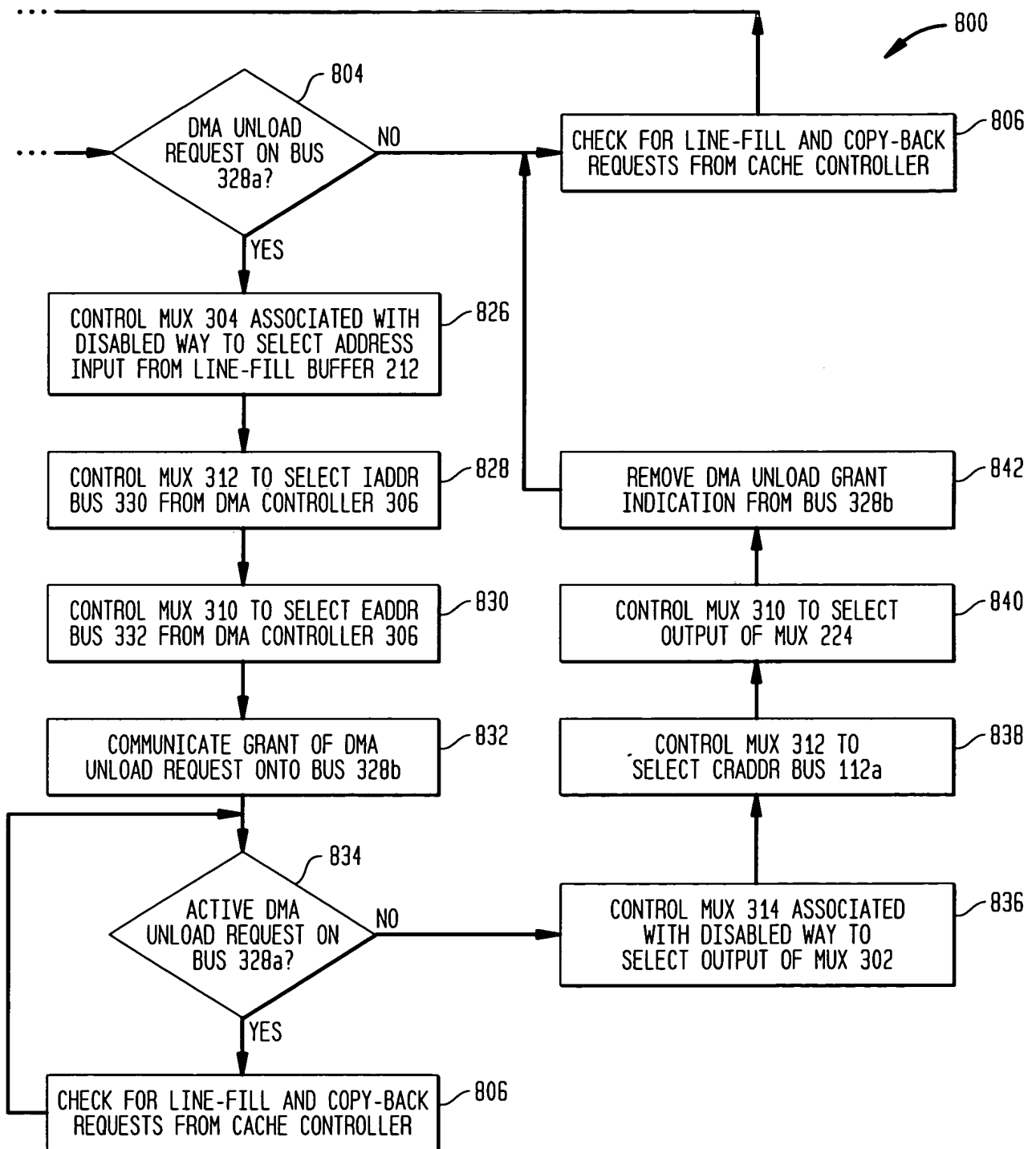
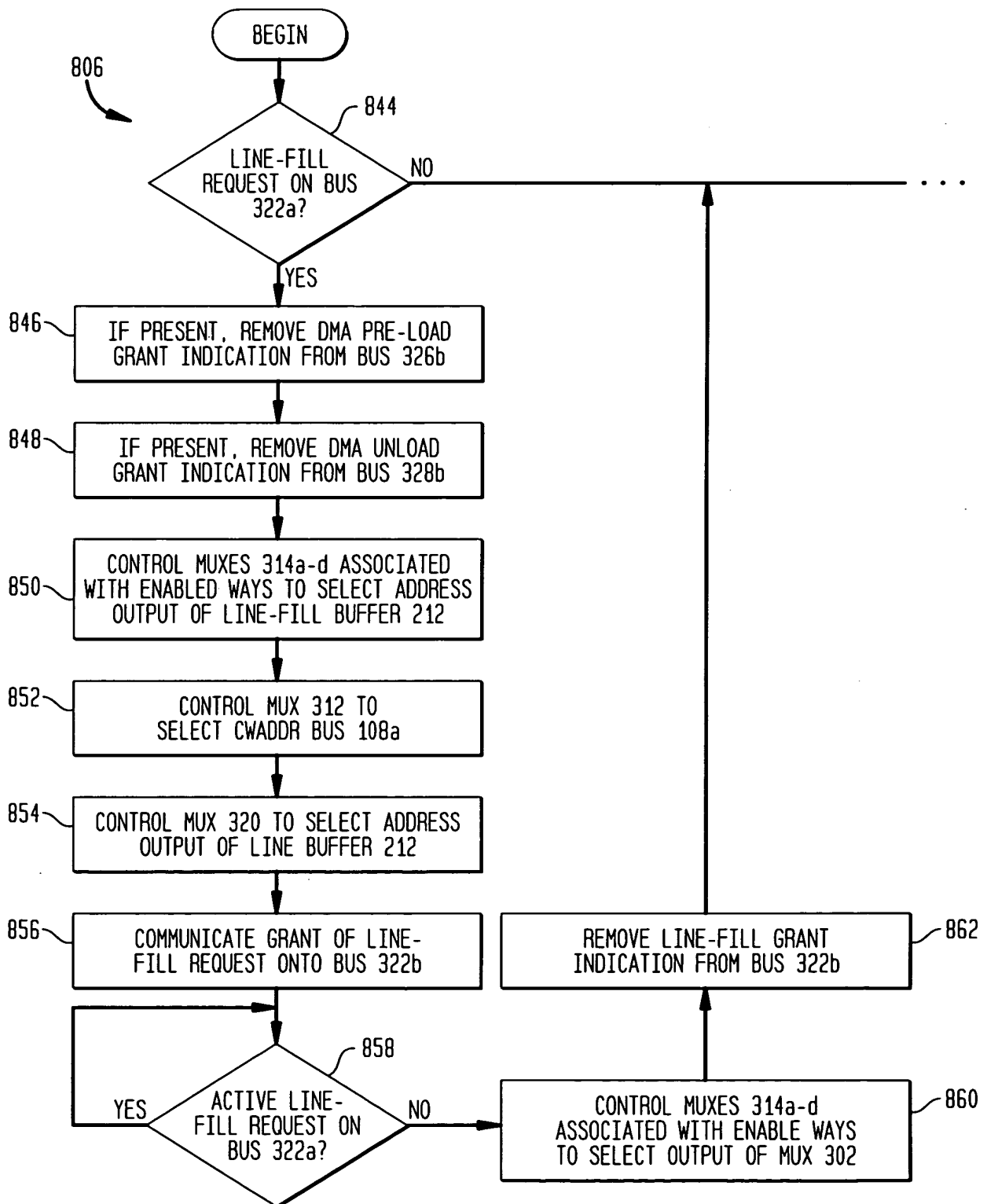


FIG. 8A2



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FIG. 8B1



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FIG. 8B2

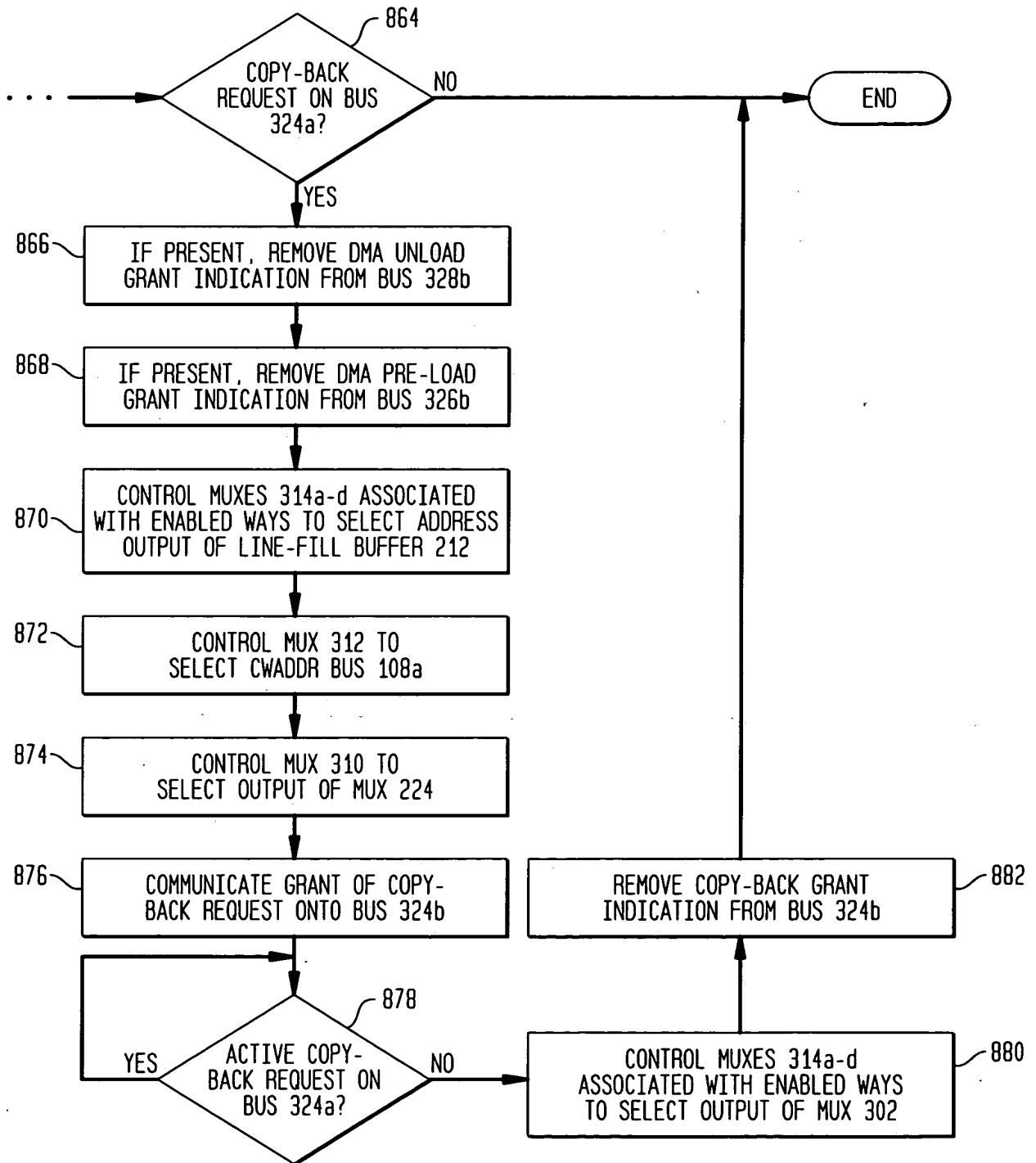


FIG. 9

